THE INVENTION CLAIMED IS:

1. A method for manufacturing an integrated circuit structure, comprising:

providing a semiconductor substrate;

forming a thyristor having at least four layers with three P-N junctions therebetween, at least two of the layers being formed horizontally on the semiconductor substrate and at least two of the layers being formed vertically on the semiconductor substrate;

forming a gate adjacent at least one of the vertically formed layers;

forming an access transistor on the semiconductor substrate; and

forming an interconnect between the thyristor and the access transistor.

2. The method of claim 1 wherein providing the semiconductor substrate includes providing a semiconductor-on-insulator substrate.

3. The method of claim 1 wherein forming the thyristor includes forming at least two of the vertical layers in a vertical pillar on the semiconductor substrate.

4. The method of claim 3 wherein forming the gate includes forming a surround gate around the vertical pillar.

5. The method of claim 3 wherein forming the interconnect includes forming a local interconnect above the semiconductor substrate connecting the pillar and the access transistor.

6. A method for manufacturing an integrated circuit structure, comprising:

providing an underlying silicon semiconductor substrate;

forming a layer of buried silicon oxide on the underlying silicon semiconductor substrate;

forming an upper layer of silicon on the layer of buried silicon oxide;

implanting N- and P- regions in the upper layer of silicon;

depositing at least one additional layer on the upper layer of silicon;

etching the additional layer to form a hole therein over the N- implantation region;

growing a vertical P-type silicon pillar in the hole by selective epitaxy;

stripping off the additional layer;

growing gate oxide around the sides of the P- Si pillar and over the P- implantation region;

forming a polysilicon gate over the gate oxide in the P- implantation region;

forming and implanting a polysilicon gate adjacent the P- Si pillar;

implanting N- source/drain areas adjacent the polysilicon gate over the P- implantation region;

depositing nitride spacers around at least one of the polysilicon gates and the P- Si pillar;

forming N+ implantations in the N- source/drain areas, in the top of the P- Si pillar, and in the top of the polysilicon gate over the P- implantation region;

forming a P+ implantation in the N- implantation adjacent the P- Si pillar, using the nitride spacer around the P- Si pillar to self-align the P+ implantation thereadjacent;

forming respective salicide layers over the N+ and P+ implantations; and

forming an interconnect between the salicide layer over the top of the P- Si pillar and one of the salicide layers over the N- source/drain areas.

7. The method of claim 6 wherein forming the gate adjacent the P- Si pillar includes forming a surround gate around the vertical P- Si pillar.

8. The method of claim 6 further comprising activating the implantations by rapid thermal anneal.

9. The method of claim 6 wherein forming the interconnect includes forming a local interconnect above the semiconductor substrate.

10. The method of claim 6 further comprising:

depositing an interlayer dielectric; and

forming electrical contacts through the interlayer dielectric to a plurality of the salicide layers.

11. An integrated circuit structure, comprising:

a semiconductor substrate;

a thyristor having at least four layers with three P-N junctions therebetween, at least two of the layers being formed horizontally on the semiconductor substrate and at least two of the layers being formed vertically on the semiconductor substrate;

a gate adjacent at least one of the vertically formed layers;

an access transistor on the semiconductor substrate; and

an interconnect between the thyristor and the access transistor.

12. The integrated circuit structure of claim 11 wherein the semiconductor substrate is a semiconductor-on-insulator substrate.

13. The integrated circuit structure of claim 11 wherein at least two of the vertical layers form a vertical pillar on the semiconductor substrate.

14. The integrated circuit structure of claim 13 wherein the gate is a surround gate around the vertical pillar.

15. The integrated circuit structure of claim 13 wherein the interconnect is a local interconnect above the semiconductor substrate connecting between the pillar and the access transistor.

16. An integrated circuit structure, comprising:

a silicon semiconductor substrate;

N- and P- implanted regions in the silicon semiconductor substrate;

a vertical P-type silicon pillar;

gate oxide around the sides of the P- Si pillar and over the P- implantation region;

a polysilicon gate over the gate oxide in the P- implantation region;

an implanted polysilicon gate adjacent the P- Si pillar;

implanted N- source/drain areas adjacent the polysilicon gate over the P- implantation region;

nitride spacers around at least one of the polysilicon gates and the P- Si pillar;

N+ implantations in the N- source/drain areas, in the top of the P- Si pillar, and in the top of the polysilicon gate over the P- implantation region;

a self-aligned P+ implantation in the N- implantation adjacent the P- Si pillar;

respective salicide layers over the N+ and P+ implantations; and

an interconnect between the salicide layer over the top of the P- Si pillar and one of the salicide layers over the N- source/drain areas.

17. The integrated circuit structure of claim 16 wherein the silicon semiconductor substrate further comprises:

an underlying silicon semiconductor substrate;

a layer of buried silicon oxide on the underlying silicon semiconductor substrate; and

an upper layer of silicon on the layer of buried silicon oxide.

18. The integrated circuit structure of claim 16 wherein the gate adjacent the P- Si pillar is a surround gate around the vertical P- Si pillar.

19. The integrated circuit structure of claim 16 wherein the interconnect is a local interconnect above the semiconductor substrate.

20. The integrated circuit structure of claim 16 further comprising:

an interlayer dielectric; and

electrical contacts through the interlayer dielectric to a plurality of the salicide layers.